Claims:

1. A system to initiate, by a host, an event in a first device, the system comprising:

a signal line to communicate a plurality of data values between a host and one or more

second devices; and

a tap line to communicate said plurality of data values between said signal line and said

first device;

wherein said event is initiated upon detection, by said first device, of a predetermined

sequence of data values on the tap line.

2. The system of claim 1, wherein the event comprises a switching from a communication

path between the first device and a third device and a communication path between the signal

line and the third device.

3. The system of claim 1, wherein the event comprises a switching from a communication

path between a signal line and a third device and a communication path between the first device

and the third device.

4. The system of claim 1, wherein the host is a processor.

5. The system of claim 1, wherein the first device is a logic device.

6. The system of claim 1, wherein each of the one or more second devices is a memory

device.

1   7.   The system of claim 1, wherein the third device is a memory device.

1   8.   The system of claim 1, wherein the host is a microprocessor chipset, the first device is a

2   Field Programmable Gate Array (FPGA), each of the one or more second devices is a Dual In-

3   line Memory Module (DIMM), and the third device is Synchronous Dynamic Random Access

4   Memory (SDRAM).

1   9.   The system of claim 1, wherein each of the plurality of data values represents a memory

2   location within any of the plurality of second memory devices.

1   10.   The system of claim 9, wherein utilization of a data value provides a call to the

2   represented memory location.

1   11.   A method to initiate, by a host, an event in a first device comprising:

2   communicating, by a signal line, a plurality of data values between a host and one or

3   more second devices;

4   communicating, by a tap line, said plurality of data values between said signal line and

5   said first device; and

6   initiating said event upon detection by said first device of a predetermined sequence of

7   data values on the tap line.

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1 12.   The method of claim 11, wherein the event comprises a switching from a communication

2 path between the first device and a third device and a communication path between the signal

3 line and the third device.

1 13.   The method of claim 11, wherein the event comprises a switching from a communication

2 path between a signal line and a third device and a communication path between the first device

3 and the third device.

1 14.   The method of claim 11, wherein the host is a processor.

15.   The method of claim 11, wherein the first device is a logic device.

16.   The method of claim 11, wherein each of the one or more second devices is a memory

device.

1 17.   The method of claim 11, wherein the third device is a memory device.

1 18.   The method of claim 11, wherein the host is a microprocessor chipset, the first device is a

2 Field Programmable Gate Array (FPGA), each of the one or more second devices is a Dual In-

3 line Memory Module (DIMM), and the third device is Synchronous Dynamic Random Access

4 Memory (SDRAM).

1   19.   The method of claim 11, wherein each of the plurality of data values represents a memory

2   location within any of the plurality of second memory devices.

1   20.   The method of claim 19, wherein utilization of a data value provides a call to the

2   represented memory location.

1   21.   A set of instructions residing in a storage medium, said set of instructions capable of

2   being executed by a processor to initiate, by a host, an event in a first device comprising:

3   communicating, by a signal line, a plurality of data values between a host and one or

4   more second devices;

5   communicating, by a tap line, said plurality of data values between said signal line and

6   said first device; and

7   initiating said event upon detection by said first device of a predetermined sequence of

8   data values on the tap line.

1   22.   The set of instructions of claim 21, wherein the event comprises a switching from a

2   communication path between the first device and a third device and a communication path

3   between the signal line and the third device.

1   23.   The set of instructions of claim 21, wherein the event comprises a switching from a

2   communication path between a signal line and a third device and a communication path between

3   the first device and the third device.

1   24.   The set of instructions of claim 21, wherein the host is a processor.

1   25.   The set of instructions of claim 21, wherein the first device is a logic device.

1   26.   The set of instructions of claim 21, wherein each of the one or more second devices is a

2   memory device.

1   27.   The set of instructions of claim 21, wherein the third device is a memory device.

1   28.   The set of instructions of claim 21, wherein the host is a microprocessor chipset, the first

2   device is a Field Programmable Gate Array (FPGA), each of the one or more second devices is a

3   Dual In-line Memory Module (DIMM), and the third device is Synchronous Dynamic Random

4   Access Memory (SDRAM).

1   29.   The set of instructions of claim 21, wherein each of the plurality of data values represents

2   a memory location within any of the plurality of second memory devices.

1   30.   The set of instructions of claim 29, wherein utilization of a data value provides a call to

2   the represented memory location.